DATA SHEET

SUNPLUS

SPLC564A

High-Voltage Durable 240-Channel Common Driver for Dot-Matrix STN LCD

MAY. 16 2005

Version: 1.1

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HIGH-VOLTAGE DURABLE 240-CHANNEL COMMON DRIVER FOR DOT-MATRIX STN LCD

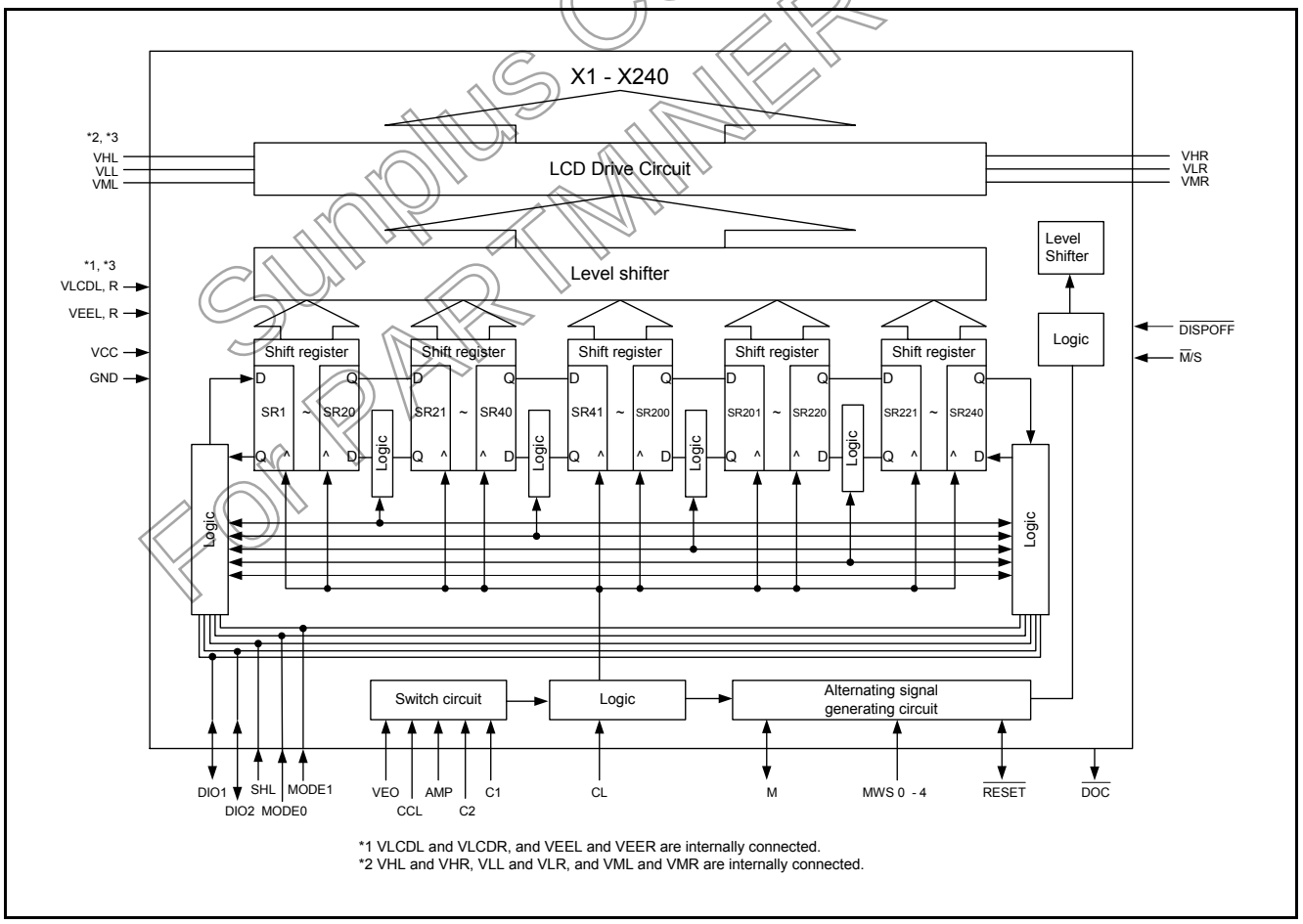
1. GENERAL DESCRIPTION

The SPLC564A is a 240-channel common driver which drives a dot matrix STN LCD panel. By changing the mode, this can be applied to 240- and 200- and 160-channel output. Through the use of a 43V high-voltage CMOS process technology, a high-voltage drive of +21.5V and -21.5V, centering on VM is possible. -21.5V generated from +21.5V with built-in switching circuit and external capacity. Low logic-drive voltage (3.0V) is used. This device is used together with the segment driver SPLC563A.

2. FEATURES

- Display duty: Up to 1/240
- LCD drive voltage: 43V max
- Built-in switching circuit (to generate -21.5V)
- Number of LCD drive circuit: 240
- Operating voltage: 2.5V to 5.5V
- Intermediate voltage I/F
- Built-in alternating signal generation circuit Pin programmable
- Output mode change: 240-output mode
  200-output mode
  160-output mode
- Built-in display-off function
- Flex TCP

3. BLOCK DIAGRAM



*1 VLCDL and VLCDR, and VEEL and VEER are internally connected.
*2 VHL and VHR, VLL and VLR, and VML and VMR are internally connected.

3.1. Internal Block Diagram

3.1.1. LCD drive circuit

This circuit selects and outputs the three level signals for the LCD drive. By a combination of the data in the shift register and M, either VH, VL, or VM is selected and transmitted to the output circuit.

3.1.2. Level shifter

This boosts a 2.5V - 5.5V signal to a high-voltage signal for LCD drive.

3.1.3. Shift register

This is a 240-bit bidirectional shift register circuit. The first line marker signal output from the DIO1, pin and DIO2 pin is sequentially shifted by shift clock CL. The shift direction is determined by the SHL pin.

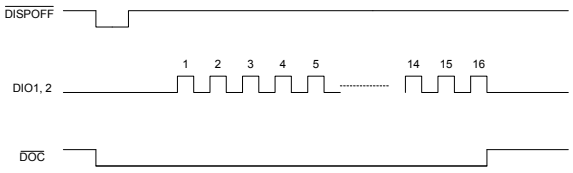
3.1.4. Alternating signal generating circuit

This circuit generates an alternating signal (M signal) for LCD display. To suppress cross-talk, the signal is alternated in a unit from several lines to several tens of lines. By connecting MWS0 to MWS4 pins to VCC or GND, the desired number of signals can be alternated. When alternating signals are externally input, all pins (MWS0 to MWS4) are connected to GND.

4. SIGNAL DESCRIPTIONS

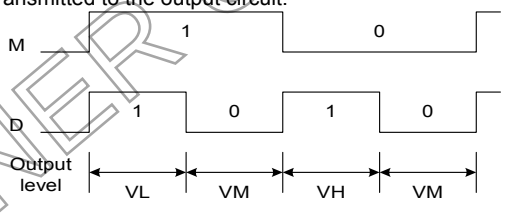
<table>
<tr><th>Classification</th><th>Symbol</th><th>PIN No.</th><th>Connected to</th><th>I/O</th><th>Functions</th></tr>
<tr><td rowspan="5">Power supply</td><td>VLCDL
VLCDR
VEEL
VEER
VCC, GND</td><td>238
286
243
281
265 276</td><td>Power supply</td><td>-</td><td>VLCDL, VLCDR–VEEL, VEER: Power supply for LCD drive
VLCDL, VLCDR: Power supply for switch circuit
VCC –GND: Power supply for logic circuit</td></tr>
<tr><td>VHL
VHR
VLL
VHR
VML
VMR</td><td>239
285
242
282
240, 241
284, 283</td><td>Power supply</td><td>Input</td><td>Power supply for LCD drive level
VHL, VHR: Selected level (Set to the same voltage as VLCDL, VLCDR.)
VLL, VLR: Selected level (Set to the same voltage as VEEL, VEER.)
VML, VMR: Non-selected level</td></tr>
<tr><td>VEO</td><td>244, 245</td><td>VEEL, R</td><td>Output</td><td>When use built-in switching circuit and generate VEE, VEO pin connect to VEEL, VEER pins. VM voltage is point of reference and reversed and output the voltage input to the voltage between VLCD and VM. If built-in switching circuit is not used, don't connect any lines to this pin.</td></tr>
<tr><td>C1
C2</td><td>246, 247
248, 249</td><td>Capacitance</td><td>-</td><td>External capacitance should be connected here when using the switch circuit for generate VEE.
If built-in switching circuit is not used, don't connect any lines to this pin.</td></tr>
<tr><td rowspan="3">Control signal</td><td>CL</td><td>277</td><td>MPU</td><td>Input</td><td>Shift clock input. Data is shifted at the falling edge of shift clock CL of the shift register.</td></tr>
<tr><td>M</td><td>252</td><td>Extension driver or MPU</td><td>I/O</td><td>Inputs or outputs the alternating current for LCD drive output.</td></tr>
<tr><td>MWS0
MWS1
MWS2
MWS3
MWS4</td><td>264
262
260
258
256</td><td>-</td><td>Input</td><td>This pin specifies the cycle of the alternating signal (M signal) in the unit of the number of lines. The number of lines, which is an integer from 2 to 31, is specified as follows. Usually, specify the number of lines within a range from 10 to 31. When the SPLC564A is driven by an external alternating signal, specify the number of lines as zero.
<table>
<tr><th>Number of lines</th><th>MWS4</th><th>MWS3</th><th>MWS2</th><th>MWS1</th><th>MWS0</th><th>Line alternating waveform</th><th>M-pin status</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-</td><td>Input</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Prohibited</td><td rowspan="5">Output</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2 lines alternated</td></tr>
<tr><td>3</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>3 lines alternated</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>31</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>31 lines alternated</td></tr>
</table>
</td></tr>
</table>

4.1. PIN Functions (cont)

<table>
<tr><th>Class</th><th>Symbol</th><th>PIN No.</th><th>Connected to</th><th>Type</th><th>Functions</th></tr>
<tr><td rowspan="8">Control signal</td><td>MODE0
MODE1</td><td>267
266</td><td>-</td><td>Input</td><td>Switch terminals for the number of LCD drive output pins
<table>
<tr><th>MODE0</th><th>MODE1</th><th>Shift direction</th></tr>
<tr><td>"H"</td><td>"H"</td><td>240-output (X1, X2, X3.....X238, X239, X240)</td></tr>
<tr><td>"H"</td><td>"L"</td><td>200-output (X21, X22, X23.....X218, X219, X220)</td></tr>
<tr><td>"L"</td><td>"H"</td><td>160-output (X41, X42, X43.....X198, X199, X200)</td></tr>
<tr><td>"L"</td><td>"L"</td><td>Prohibited</td></tr>
</table></td></tr>
<tr><td>DIO1
DIO2</td><td>280
250</td><td>Extension driver or MPU</td><td>I/O</td><td>Serial data input output pin
<table>
<tr><th>SHL</th><th>DIO1</th><th>DIO2</th></tr>
<tr><td>"H" level</td><td>Serial output pin</td><td>Serial iutput pin</td></tr>
<tr><td>"L" level</td><td>Serial iutput pin</td><td>Serial output pin</td></tr>
</table></td></tr>
<tr><td>CCL</td><td>278</td><td>MPU</td><td>Input</td><td>Built-in switching circuit clock input. When use built-in switching circuit and generate VEE, this pin connect CL pin.
If built-in switching circuit is not used, CCL must be fixed to GND.</td></tr>
<tr><td>AMP</td><td>273</td><td>-</td><td>Input</td><td>Built-in switching circuit on-off control.
When use built-in switching circuit, this pin must be fixed to VCC. If built-in switching circuit is not used, this pin must be fixex to GND.</td></tr>
<tr><td>$\overline{\text{RESET}}$</td><td>254</td><td>MPU or VCC</td><td>Input</td><td>Setting this pin to GND sets initializes the alternating signal (M signal) circuit. A VCC level $\overline{\text{RESET}}$ is normally used.</td></tr>
<tr><td>$\overline{\text{DISPOFF}}$</td><td>271</td><td>MPU</td><td>Input</td><td>Setting this pin to GND sets LCD drive output X1 to X240 to the VM level.</td></tr>
<tr><td>$\overline{\text{M/S}}$</td><td>279</td><td>-</td><td>Input</td><td>Controls the display-off function, and display-off signal output from $\overline{\text{DOC}}$ pin.</td></tr>
<tr><td>$\overline{\text{DOC}}$</td><td>269</td><td>-</td><td>Output</td><td>$\overline{\text{M/S}}$ $\overline{\text{DOC}}$
"H" level When $\overline{\text{DISPOFF}}$ is low level, output low level
When $\overline{\text{DISPOFF}}$ is high level, output high level
"L" level Until serial data input 16 times output low level from $\overline{\text{DOC}}$ pin
 

When using $\overline{\text{M/S}}$ is low level, $\overline{\text{DOC}}$ pin should be connect to SEG LSI Dispoff control pin.</td></tr>
</table>

<table>
<tr><th>Class</th><th>Symbol</th><th>PIN No.</th><th>Connected to</th><th>Type</th><th>Functions</th></tr>
<tr><td></td><td>SHL</td><td>275</td><td>-</td><td>Input</td><td>This pin switches shift directions.
<table>
<tr><th>SHL</th><th>MODE0</th><th>MODE1</th><th>Shift direction</th></tr>
<tr><td rowspan="4">"H" level</td><td></td><td></td><td>Right shift</td></tr>
<tr><td>"H"</td><td>"H"</td><td>DIO2->SR1->.....->SR240->DIO1</td></tr>
<tr><td>"H"</td><td>"L"</td><td>DIO2->SR21->.....->SR220->DIO1</td></tr>
<tr><td>"L"</td><td>"H"</td><td>DIO2->SR41->.....->SR200->DIO1</td></tr>
<tr><td rowspan="4">"L" level</td><td></td><td></td><td>Left shift</td></tr>
<tr><td>"H"</td><td>"H"</td><td>DIO1->SR240->.....->SR1->DIO2</td></tr>
<tr><td>"H"</td><td>"L"</td><td>DIO1->SR220->.....->SR21->DIO2</td></tr>
<tr><td>"L"</td><td>"H"</td><td>DIO1->SR200->.....->SR41->DIO2</td></tr>
</table>
SR1, SR2···SR240 correspond to X1, X2···X240.

Note: The 40 or 80 pins invalidated at the 200-output or 160-output mode output the non- selected level synchronized every time; release these pins.</td></tr>
<tr><td>LCD drive output</td><td>X1 to X12
X13 to x220
X221 to X234
X235 to X240</td><td>236 - 225
223 - 16
14 - 1
292 - 287</td><td>LCD</td><td>Output</td><td>LCD drive output
By a combination of the display data and the M signal, when DISPOFF is set to VCC, either VH, VL, or VM is selected and transmitted to the output circuit.
 

Note: VH = VHL = VHR
VL = VLL = VLR
VM = VML = VMR</td></tr>
</table>

Note1: Configuring the LCD panel using the SPLC564A when using the selected SEGMENT driver.

5. ELECTRICAL SPECIFICATIONS

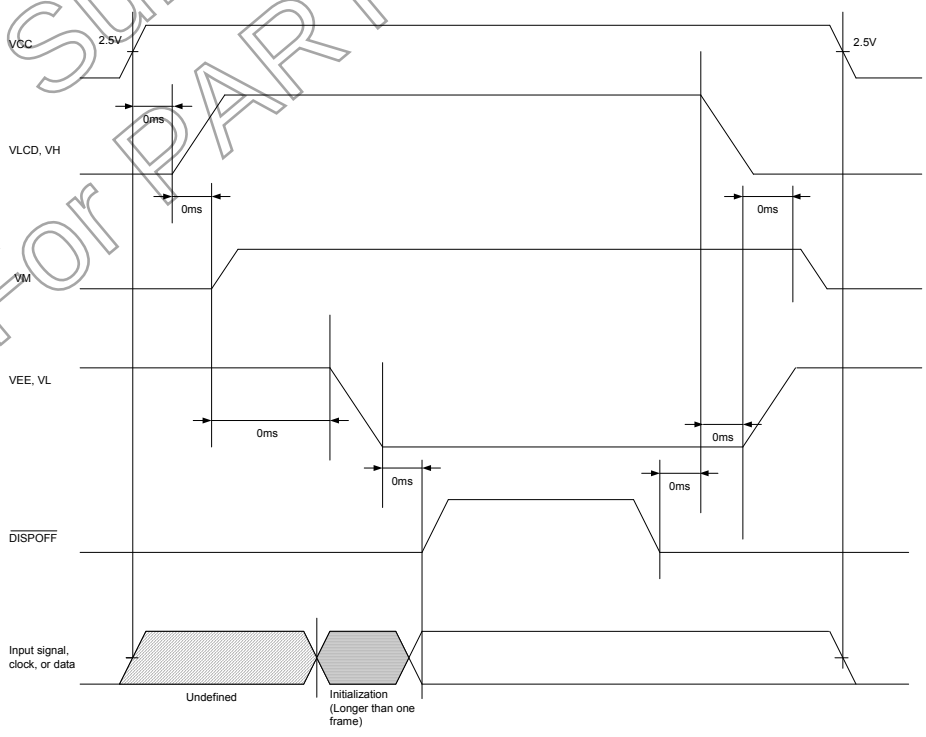
5.1. Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	VCC	– 0.3 to + 7.0	V	1, 8
Power supply voltage for LCD drive circuits	VLCD	– 0.3 to + 25	V	1, 3, 8
	VEE	– 20 to + 0.3	V	1, 4, 8
Input voltage 1	VT1	– 0.3 to VCC + 0.3	V	1, 2
Input voltage 2	VH	– 0.3 to V_{LCD}	V	1, 5, 8
Input voltage 3	VL	+ 0.3 to VEE	V	1, 6, 8
Input voltage 4	VM	– 0.3 to + 5.0	V	1, 7, 8
Operating temperature	T_{OPR}	– 30 to +75	°C	
Storage temperature	T_{STG}	– 55 to +110	°C	

Notes: If the LSI is used beyond the above maximum ratings, it may be permanently damaged.
It should always be used within its specified operating range for normal operation to prevent malfunction or degraded reliability.

Note: 1. Voltage from GND

2. Applicable to DIO1, $\overline{DISPOFF}$, SHL, M, NWS0, NWS1, NWS2, NWS3, NWS4, $\overline{RESET}$, MODE0, MODE1, CL, M/$\overline{S}$, AMP, CCL, DIO2
3. Applicable to V_{LCDL}, R pins.
4. Applicable to V_{EEL} , R pins.
5. Applicable to V_{HL}, R pins.
6. Applicable to V_{LL}, R pins.
7. Applicable to V_{ML}, R pins.
   (Caution)
   Operating the LSI in excess of the absolute maximum rating will result in permanent damage.
   Use the LSI observing electrical characteristic conditions in normal operation. Exceeding the conditions will cause malfunctions or will affect LSI reliability.
8. Observe the sequence of activation and inactivation for the following power supplies and signals.
   And this sequence apply to use built-in switching circuit.
   If the sequence is not observed, it may cause LSI malfunction, permanent damage, or adverse effects.



5.1.1. Power ON

1). Turn on the power supply in the order of GND - VCC, GND -VLCD (VH), and VM. VM-VEE is generated automatically. In this case, input GND to the $\overline{\text{DISPOFF}}$ pin.

2). The LCD level forcibly outputs the VM level by the DISPOFF function.

3). The DISPOFF function has a priority even if input signal distortion occurs immediately after VCC input.

4). Then input the predetermined signals to initialize the driver registers. In this case, assure a period for more than one frame.

5). Preparation for normal display is thus completed. Cancel the DISPOFF function by setting the $\overline{\text{DISPOFF}}$ pin to VCC. At this point, the levels of VEE (VL), VLCD (VH) and VM must has reached the predetermined respective voltage.

5.1.2. Shut down

As a rule, shut down in order opposite to that used for power on.

1). Set the $\overline{\text{DISPOFF}}$ pin to GND.

2). At first shut off the LCD power supply GND-VLCD (VH), at same time GND-VEE (VL) get to VM. Next shut off the VM.

3). Set VCC and the input signal to GND.

At this point, VEE (VL), VLCD (VH) and VM pin input must completely drop to 0V.

Since the DISPOFF function is inactivated when the VCC level drops to GND, the LCD output may output a level other than VM. Therefore, an incorrect display may appear at shut down or power on.

5.2. DC Characteristics 1

(VCC = 2.5V to 5.5V, GND = 0V, VLCD - VEE = 15V to 43V, T_A = -30℃ to +75℃)

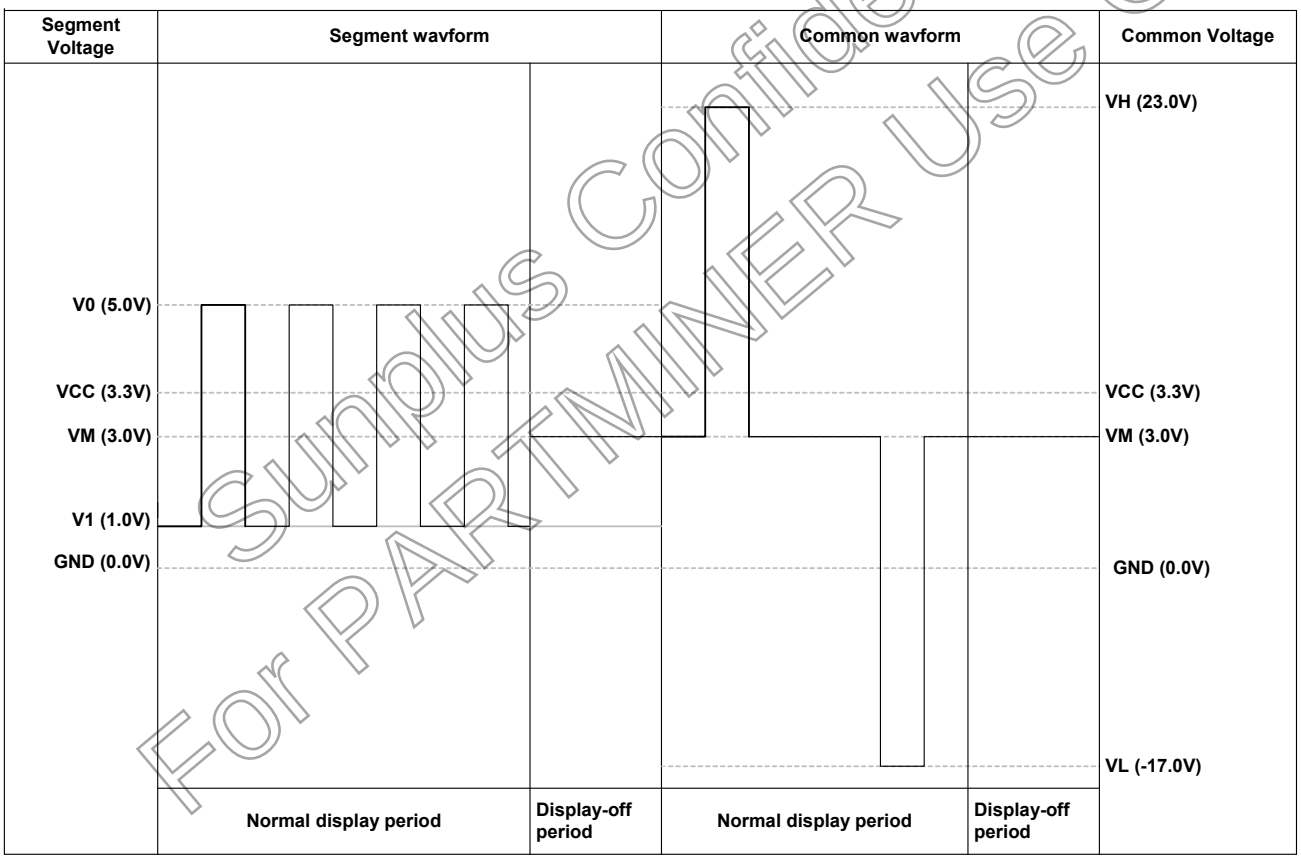
Item	Symbol	PINs	Min.	Typ.	Max.	Unit	Test Condition	Notes
Input high voltage	V_{IH}	DIO1, $\overline{\text{DISPOFF}}$, SHL, M, $\overline{\text{M/S}}$, MWS0-4, $\overline{\text{RESET}}$	0.7 x VCC	-	VCC	V		
Input low voltage	V_{IL}	CL, MODE0, MODE1, $\overline{\text{DOC}}$, AMP, CCL, DIO2	0	-	0.3 x VCC	V		
Output high-level voltage	V_{OH}	M, $\overline{\text{DOC}}$, DIO1, DIO2	VCC - 0.4	-	-	V	I_{OH} = -0.4mA	
Output low-level voltage	V_{OL}	M, $\overline{\text{DOC}}$, DIO1, DIO2	-	-	0.4	V	I_{OL} = 0.4mA	
ON resistance between Vi - Yj	R_{ON}	X1 to X240, V pin	-	0.7	2.0	KΩ	I_{ON} = 150μA	1
Input leakage current (1)	I_{IL1}	DIO1, $\overline{\text{DISPOFF}}$, SHL, M, $\overline{\text{M/S}}$, MWS0-4, $\overline{\text{RESET}}$, CL, MODE0, MODE1, $\overline{\text{DOC}}$, AMP, CCL, DIO2	-5.0	-	5.0	μA	VIN = VCC to GND	
Input leakage current (2)	I_{IL2}	VH, VL, VM, C1, C2	-25	-	25	μA		
Input leakage consumption (1)	I_{CC1}	VCC	-	10	40	μA	VCC = 3.3V, VLCD - VEE = 40V, fCL = 19.2KHz, fM = 1.5KHz	2

Item	Symbol	PINs	Min.	Typ.	Max.	Unit	Test Condition	Notes
Current consumption (2)	I_{CC2}	VCC	-	20	50	μA	VCC = 5.0V, VLCD - VEE = 40V, fCL = 19.2KHz, fM = 1.5KHz	
Current consumption (3)	I_{LCD}	V_{LCD}	-	25	50	μA	VCC = 3.3V, VLCD - VEE = 40V, fCL = 19.2KHz, fM = 1.5KHz	

Note1: This is a resistance value between the X and V pins (either of VH, VL, or VM) when a load current is applied to one of X1 to X240 pins. These values are regulated under the conditions of VLCD = VH = 21.75V, VEE = VL = -18.5V, VM = 1.75V, GND = 0V, Use VH, VL, and VM in the range of VLCD - VM≧VH-VM = 21.5 to 7.5V, VEE - VM≦VL - VM = -21.5 to -7.5V, with the relation of VH > VM > VL.

Note2: The current applied between the input and output is excluded. When an input to a CMOS gate is at an intermediate level, through current flows between the power supplies and the power supply current increases. Therefore, use V_{IH} = VCC and V_{IL} = GND.

Note3: The voltage relationship of each signal is as follows:



5.3. AC Characteristics 1

(VCC = 2.5V to 5.5V, GND = 0V, VLCD - VEE = 15V to 43V, T_A = -30°C to +75°C)

Item	Symbol	PINs	Min.	Max.	Unit	Note
Clock cycle time	tCYC	CL	400	-	ns	
Clock high-level width	tCWH	CL	25	-	ns	
Clock low-level width	tCWL	CL	370	-	ns	
CL rising time	tr	CL	-	30	ns	
CL falling time	tf	CL	-	30	ns	
Data setup time	tDS	DIO1, DIO2, CL	100	-	ns	
Data hold time	tDH	DIO1, DIO2, CL	10	-	ns	
Data output delay time	tDD	DIO1, DIO2, CL	-	200	ns	*1
M output delay time	tMD	M, CL	-	200	ns	*1
M setup time	tMS	M, CL	20	-	ns	
M hold time	tMH	M, CL	20	-	ns	
DOC delay time 1	tDOC1	$\overline{\text{DISPOFF}}$, $\overline{\text{DOC}}$	-	300	ns	*2
DOC delay time 2	tDOC2	DIO1, DIO2, $\overline{\text{DOC}}$	-	300	ns	*2

5.4. AC Characteristics 2

(VCC = 2.5V to 4.5V, GND = 0V, VLCD - VEE = 43V, T_A = -30°C to +75°C)

Item	Symbol	PINs	Min.	Max.	Unit	Note
Output delay time 1	t_{pd1}	X (n), M	-	1.2	μs	*2

5.5. AC Characteristics 3

(VCC = 4.5V to 5.5V, GND = 0V, VLCD - VEE = 43V, T_A = -30°C to +75°C)

Item	Symbol	PINs	Min.	Max.	Unit	Note
Output delay time 1	t_{pd1}	X (n), M	-	0.7	μs	*2

Notes: *1, *2. The following timing is regulated with the circuit at the right connected.

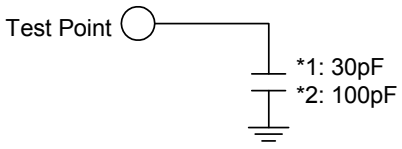
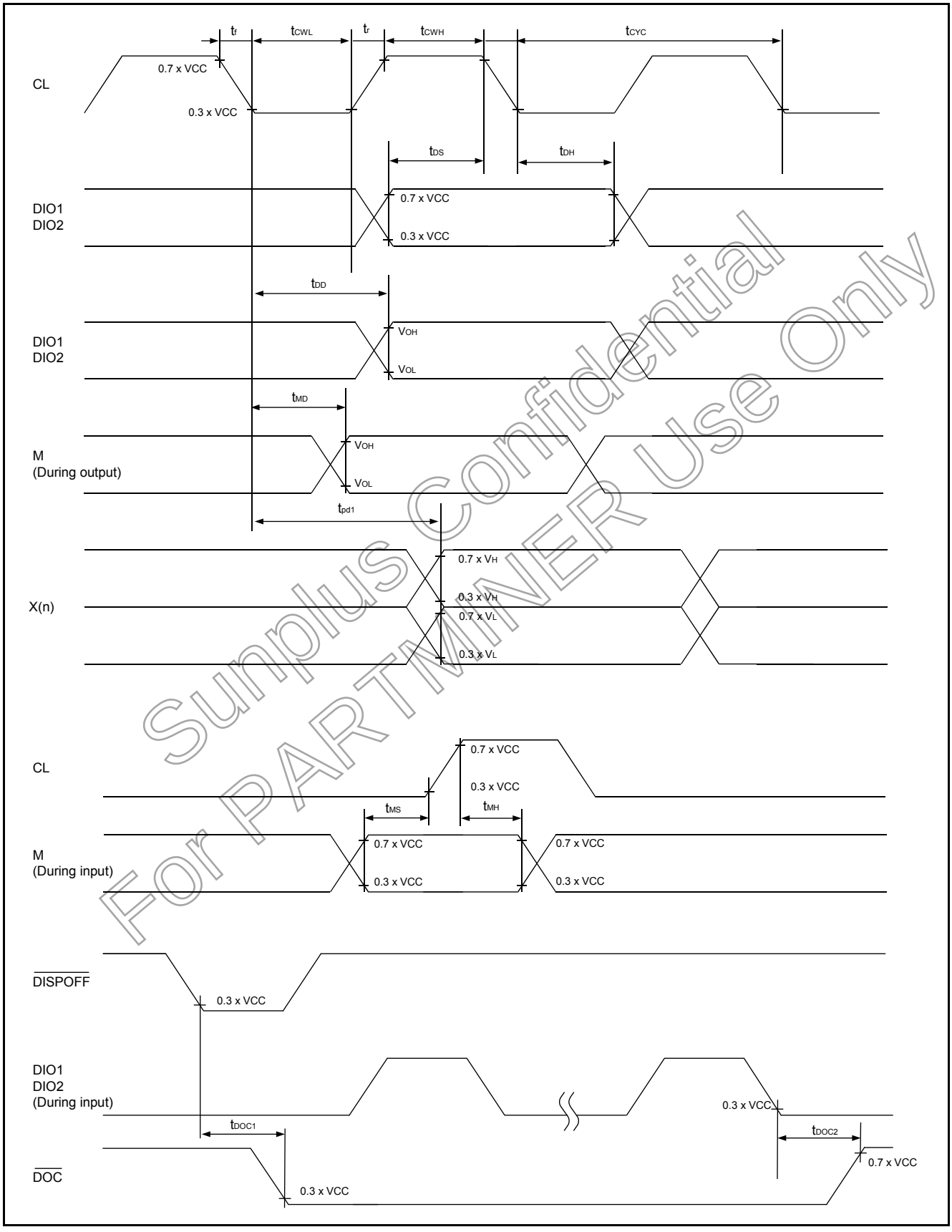
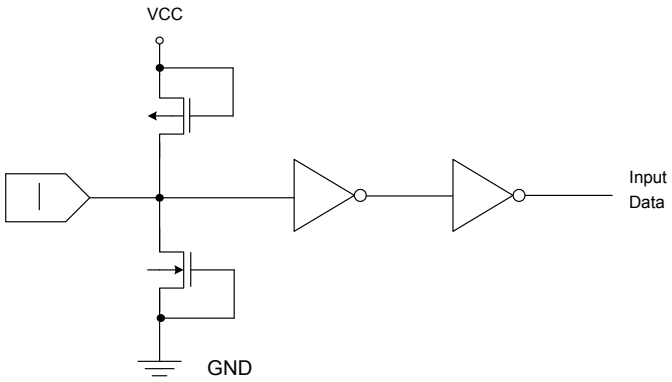


Figure 4: Load circuit

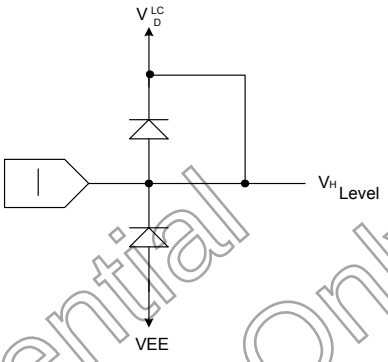


5.6. Terminal Configuration

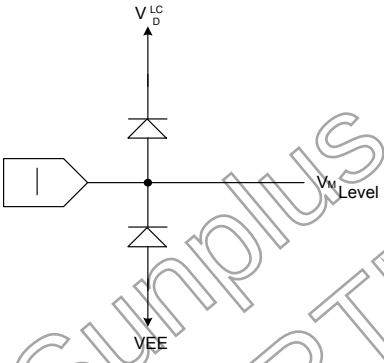
5.6.1. Terminal configuration (1)



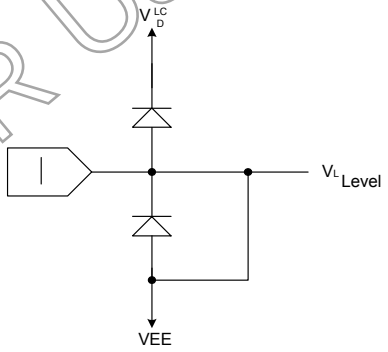
Input Terminal 1
Applicable terminals: CL, CCL, SHL, MODE0, 1, AMP
$\overline{DISPOFF}$, $\overline{RESET}$, MWS0-4, $\overline{M/S}$



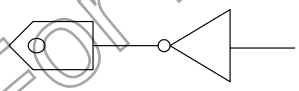
Input Terminal 3
Applicable terminals: $V_{HR, L}$
*V_{HR} terminal connect with V_{HL} terminal in LSI.



Input Terminal 2
Applicable terminals: $V_{MR, L}$
*V_{MR} terminal connect with V_{ML} terminal in LSI.

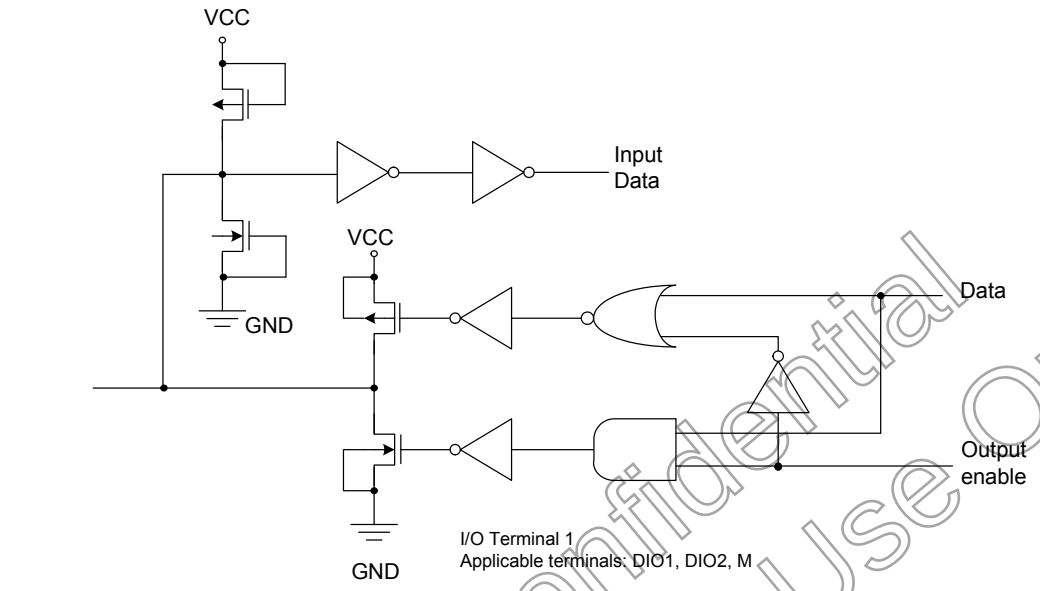


Input Terminal 2
Applicable terminals: $V_{MR, L}$
*V_{MR} terminal connect with V_{ML} terminal in LSI.

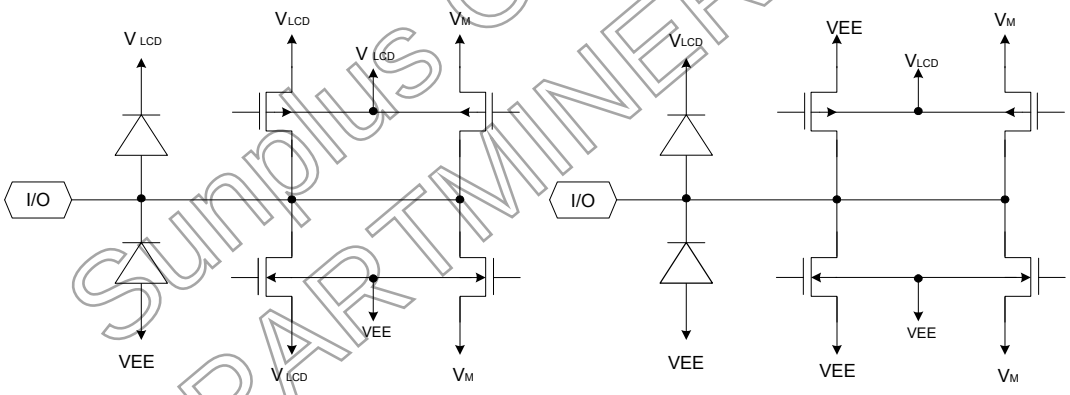


Output Terminal 1
Applicable terminals: $\overline{DOC}$

5.6.2. Terminal Configuration (2)

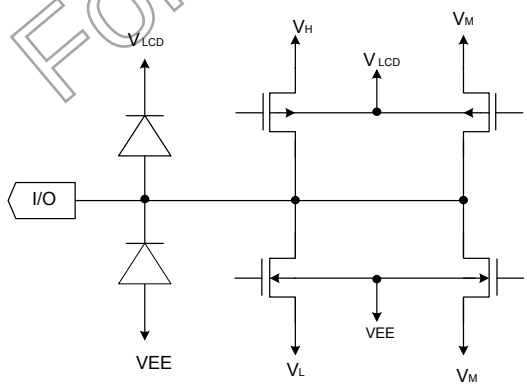


I/O Terminal 1
Applicable terminals: DIO1, DIO2, M



I/O Terminal 2
Applicable terminals: C1

I/O Terminal 3
Applicable terminals: C2



LCD drive Output Terminal
Applicable terminals: X1 to X240

6. APPLICATION CIRCUIT

6.1. Application Example

Figure 1 shows an application example 320 x 3 (collar) x 240 dot Half VGA Size STN color panel.

This panel configured SPLC564A X 1 piece and SPLC563 x 3 pieces.

SPLC564A generates M signal and DOC signal. M signal pin is connected M signal pin of SPLC563A.

SPLC564A is able to generates - voltage by external capacitor.

VEO pin is connected VEE pin and VL pin.

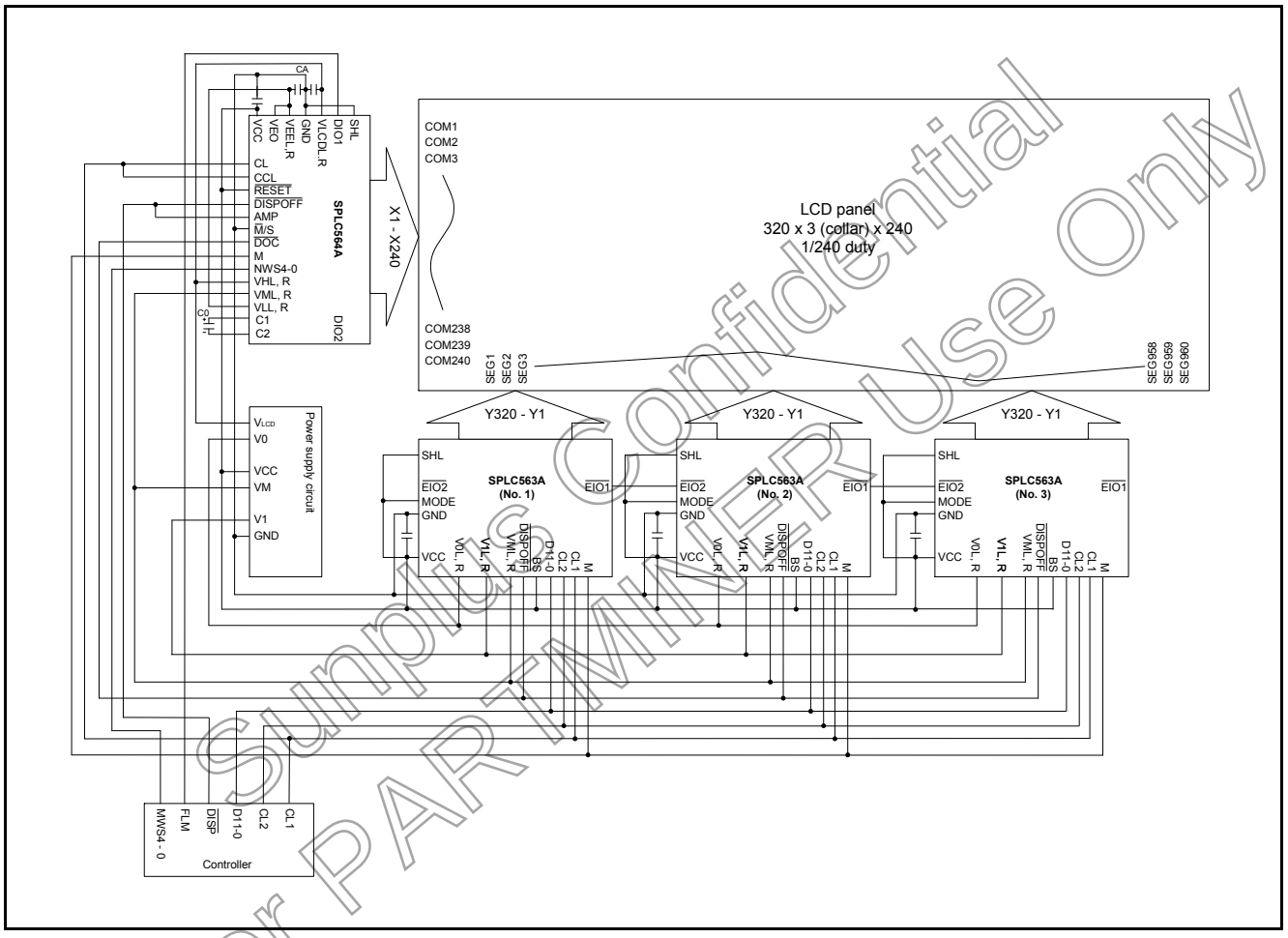


Figure 1: Application Example

Note1: When designing the board, connect a capacitor near the IC to stabilize power supply. Use two capacitors of about 0.1μF for each IC (between VCC and GND, V0 and GND, VLCD and GND, and VEE and GND)

Note2: In addition, for the power supply circuit, connect a capacitor of several μF or several tens of μF between the liquid-crystal power supply and GND. For set evaluation, confirm that there is no inversion of liquid-crystal drive power supply and level power supply in turned on and when it is turned off.

Note3: When using external capacitor to generate VEE, you must connect a capacitor of several μF or several tens of μF between the VEE and GND.

6.2. Power Supply Circuit Example

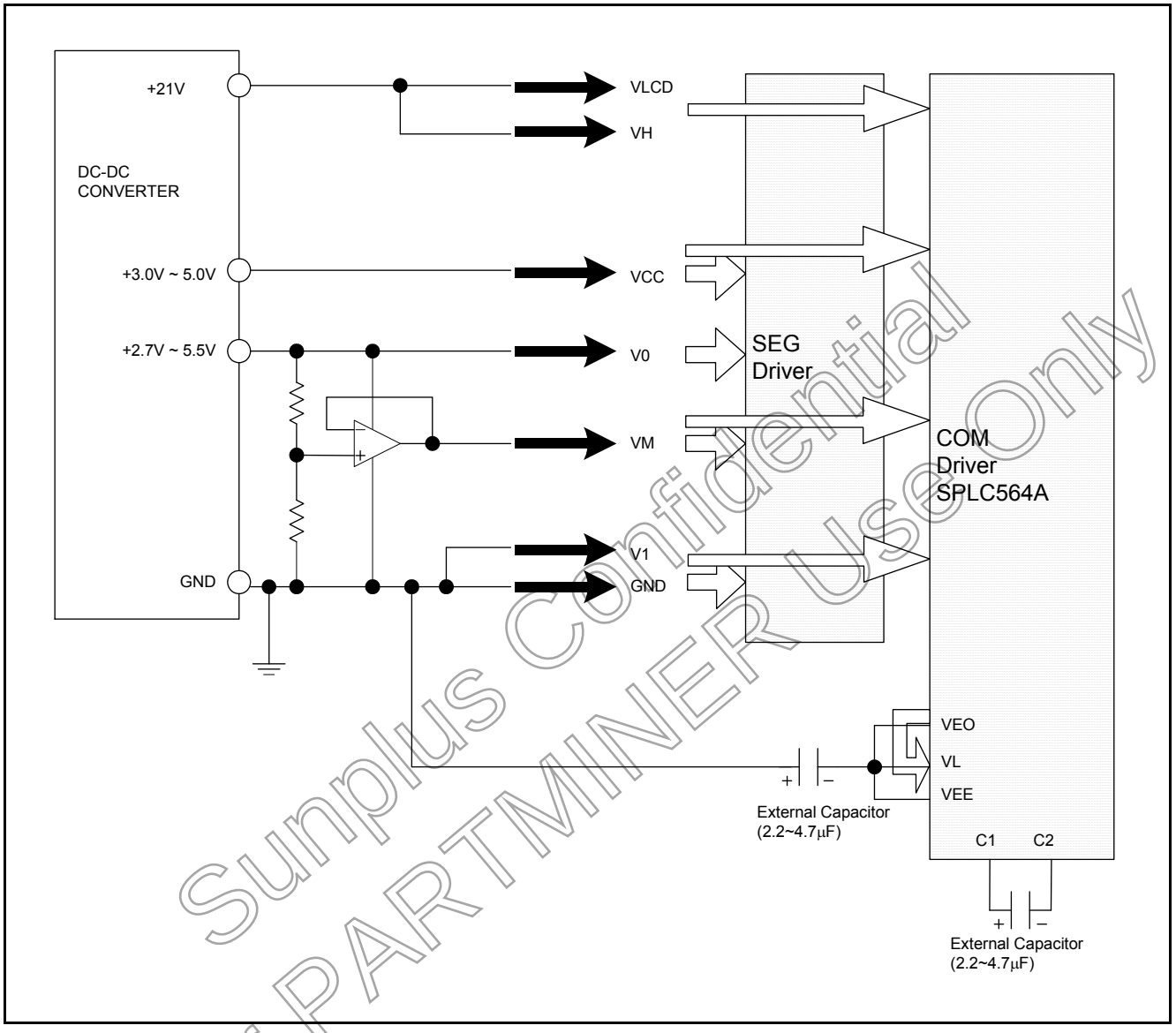


Figure 2: Power Supply Circuit Example

7. PACKAGE/PAD LOCATIONS

7.1. Package/PAD Locations

Please contact Sunplus sales representatives for more information.

7.2. Ordering Information

Product Number	Package Type
SPLC564A-C	Chip form
SPLC564A-PT112	Package form - TCP 5SP, 70W
SPLC564A-PJ061	Package form - COF 5SP, 70W

8. DISCLAIMER

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9. REVISION HISTORY

Date	Revision #	Description	Page
MAY. 16, 2005	1.1	1. Add package information “SPLC564A-PJ061” 2. Modify Terminal configuration (1) 3. Modify Terminal Configuration (2) 4. Correct PIN No. 5. Delete SPLC564A-PC011 ordering information	17 13 14 5 - 7 17
FEB. 20, 2004	1.0	1. Add package information 2. Remove “*Preliminary*”	7
JUN. 19, 2003	0.3	1. Correct “*4.2 Ordering Information*” 2. Remove “*7. PACKAGE/PAD LOCATIONS*”	7 17
JAN. 29, 2003	0.2	1. Correct type error 2. Correct “Bumped pad height”: 17 to 18	3 17
JUL. 11, 2001	0.1	Original	24